AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor package comprising:

a chip carrier including a grounded pad on a first side of said chip carrier;

a semiconductor chip coupled to said first side of said chip carrier;

a conductive lid thermally coupled to said semiconductor chip, wherein the entire length of said conductive lid is substantially parallel with said first side of said chip carrier; and

~~a discrete conductive structure~~ a conductive block having about the same dimensions as a discrete chip component, wherein ~~said discrete conductive structure~~ said conductive block is electrically coupled to said grounded pad and to said conductive lid.

2. (Currently Amended) The semiconductor package of claim 1 wherein a solder connects said conductive ~~structure~~ block and said grounded pad.

3. (Currently Amended) The semiconductor package according to claim 1 wherein said conductive ~~structure~~ block is electrically coupled to said grounded pad with an electrically conductive adhesive material.

4. (Currently Amended) The semiconductor package according to claim 1 wherein said conductive ~~structure~~ block is electrically coupled to said conductive lid with an electrically conductive adhesive material.

5. (Currently Amended) The semiconductor package according to claim 1 wherein said conductive ~~structure~~ block is coupled to said chip carrier using an electrically insulative adhesive material.

6. (Currently Amended) The semiconductor package according to claim 1 wherein said conductive ~~structure~~ block is coupled to said chip carrier using a thermally conductive adhesive material.

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Currently Amended) The semiconductor package according to claim 1 wherein
a solder couples said conductive ~~structure~~ block to said grounded pad;
an electrically conductive adhesive material couples said conductive ~~structure~~ block to said conductive lid; and
an electrically insulative adhesive material couples said conductive ~~structure~~ block to said chip carrier.

11. (Canceled)

12. (Canceled)

13. (Canceled)

Claims 14 – 21 (Canceled)

22. (Previously Presented) The semiconductor package of claim 1 wherein an end of said conductive lid extends beyond at least one side of said semiconductor chip.

23. (Currently Amended) The semiconductor package of claim 1 wherein said conductive ~~structure~~ block is located on said first side of said chip carrier.

24. (Currently Amended) The semiconductor package of claim 1 wherein said conductive ~~structure~~ block has about the same dimensions as a surface mount technology (SMT)

discrete component.

25. (Currently Amended) The semiconductor package of claim 1 wherein said conductive ~~structure~~ block occupies a substantial amount of a gap between a lower surface of said conductive lid and an upper surface of said chip carrier.

26. (Currently Amended) The semiconductor package of claim 25 wherein said conductive ~~structure~~ block occupies about 90% of said gap.

27. (New) A semiconductor package comprising:

a chip carrier including a grounded pad on a first side of said chip carrier;

a semiconductor chip coupled to said first side of said chip carrier;

a conductive lid thermally coupled to said semiconductor chip, wherein the entire length of said conductive lid is substantially parallel with said first side of said chip carrier; and

a conductive spring having about the same dimensions as a discrete chip component, wherein said conductive spring is electrically coupled to said grounded pad and to said conductive lid.

28. (New) The semiconductor package according to claim 27 wherein said conductive spring is electrically coupled to said grounded pad with an electrically conductive adhesive material.

29. (New) The semiconductor package according to claim 27 wherein said conductive spring is electrically coupled to said conductive lid with an electrically conductive adhesive material.

30. (New) The semiconductor package according to claim 27 wherein said conductive spring is coupled to said chip carrier using an electrically insulative adhesive material.

31. (New) The semiconductor package according to claim 27 wherein said conductive spring is coupled to said chip carrier using a thermally conductive adhesive material.

32. (New) The semiconductor package of claim 27 wherein said conductive spring has about the same dimensions as a surface mount technology (SMT) discrete component.

33. (New) The semiconductor package of claim 27 wherein said conductive spring occupies a substantial amount of a gap between a lower surface of said conductive lid and an upper surface of said chip carrier.